CLAIMS

What is claimed is:

1. A system comprising:

a memory including a plurality of memory banks;

a first agent adapted to access a first memory portion including a first number of said plurality of memory banks; and

a second agent adapted to access a second memory portion including a second number of said plurality of memory banks;

said first number and said second number being variable.

2. The system according to claim 1, further comprising:

a register to set at least one of said first number and said second number.

3. The system according to claim 1, wherein:

said register is adapted to be set by either one of said first agent and said second agent.

4. The system according to claim 1, wherein:

a value set in said register is adapted to correspond to said first number of said plurality of memory banks.

5. The system according to claim 1, wherein:

said second number is a remainder of said plurality of said memory banks after said first number of said plurality of memory banks.

6. The system according to claim 1, wherein:

said first agent is a first digital signal processor; and

said second agent is a second digital signal processor.

7. A system comprising:

a plurality of agents;

a shared memory block accessible by each of said plurality of agents, said shared memory block including a plurality of memory banks;

a register adapted to partition said shared memory block into a plurality of partitions, each of said plurality of partitions being accessible by a unique group of said plurality of agents.

8. The system according to claim 7, wherein:

said register is setable by at least one of said plurality of agents.

9. The system according to claim 7, wherein:

said plurality of partitions each comprise an integer number of said plurality of memory banks.

10. The system according to claim 1, wherein:

said memory is synchronous memory.

11. The system according to claim 1, wherein:

said memory is asynchronous memory.

12. The system according to claim 10, wherein:

said synchronous memory is synchronous dynamic random access memory.

13. A system for providing access to shared memory, said system comprising:

a first agent to provide a memory access clock signal to allow said first agent to access said shared memory; and

a second agent using said memory access clock signal to access to said shared memory in synchronism with said access by said first agent to said shared memory.

14. The system for providing access to shared memory according to claim 13, wherein:

said shared memory block services in turn said first agent and said second agent without a wait state therebetween.

15. The system for providing access to shared memory according to claim 13, wherein:

said shared memory block is partitioned such that said first agent has access to a first partition of said shared memory block; and

said second agent has access to a second partition of said shared memory block.

16. The system for providing access to shared memory according to claim 13, wherein:

said first agent is a first digital signal processor; and

said second agent is a second digital signal processor.

17. A method of synchronizing access from a plurality of agents to shared memory, comprising:

providing a memory access clock signal;

firstly accessing said shared memory from a first agent based on said memory access clock signal;

secondly accessing said shared memory from a second agent based on said memory access clock signal;

wherein said step of secondly accessing said shared memory follows said step of firstly accessing without a wait state therebetween.

18. The method of synchronizing access from a plurality of agents to shared memory according to claim 17, further comprising:

regenerating in said second agent said memory access clock signal.

19. The method of synchronizing access from a plurality of agents to shared memory according to claim 17, wherein:

said first agent provides said memory access clock signal.

20. A method of partitioning a shared memory, comprising:

setting a configuration register to partition said shared memory into a first plurality of memory banks and a second plurality of memory banks;

accessing said first plurality of memory banks from a first agent;

accessing said second plurality of memory banks from a second agent; and

re-partitioning said shared memory on-the-fly.

21. The method of partitioning a shared memory according to claim 20, wherein:

said step of re-partitioning is performed from said first agent.

22. Apparatus for synchronizing access from a plurality of agents to shared memory, said apparatus comprising:

means for providing a memory access clock signal;

means for firstly accessing said shared memory from a first agent based on said memory access clock signal;

means for secondly accessing said shared memory from a second agent based on said memory access clock signal;

wherein said means for second accessing accesses said shared memory without a wait state after said means for firstly accessing said shared memory accesses said shared memory.

23. Apparatus for partitioning a shared memory, said apparatus comprising:

means for setting a configuration register to partition said shared memory into a first plurality of memory banks and a second plurality of memory banks;

means for accessing said first plurality of memory banks from a first agent;

means for accessing said second plurality of memory banks from a second agent; and

means for re-partitioning said shared memory on-the-fly.